



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|-------------------------------|------------------------|
| 10/651,910 | 08/29/2003 | Sami Kalajo | 875.0124.U1(US) | 9575 |
| 29683 7590 05/21/2007 HARRINGTON & SMITH, PC 4 RESEARCH DRIVE SHELTON, CT 06484-6212 | | | EXAMINER MEHRPOUR, NAGHMEH | |
| | | | ART UNIT 2617 | PAPER NUMBER |
| | | | MAIL DATE 05/21/2007 | DELIVERY MODE PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | | |
|------------------------------|------------------------|--|---------------------|--|
| Office Action Summary | Application No. | | Applicant(s) | |
| | 10/651,910 | | KALAJO ET AL. | |
| | Examiner | | Art Unit | |
| | Naghmeh Mehrpour | | 2617 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. **Claims 1-25**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hadjichristos et al. (US Patent 6,785,521 B2) in view of Kenji (US Patent Number 4,509,101).

Regarding **claims 1, 9, 17, 20-21**, Hadjichristos teaches/method/mobile terminal a power amplifier module operable over a range of output power levels (col lines 41-67, col 2 lines 1-15), comprising:

an output transistor having an input coupled to an input node of the power amplifier module and an output coupled to an output node of the power amplifier module, the power amplifier module (col 1 lines 40-56) further comprising:

circuitry for automatically compensating a load line of the output transistor for impedance variations appearing at the output node (col 5 lines 3-14, col 6 lines 6-37). Hadjichristos fails to teach a circuit comprising: a detection circuitry for generating a first detection signal having a value that is indicative of the current flowing through the output transistor and a second detection signal having a value that is indicative of the voltage appearing at the output of the output transistor, and further comprising:

compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, and the current output power level of the power amplifier module. However, Kenji teaches a detection circuitry for generating a first detection signal having a value that is indicative of the current flowing through the output transistor and a second detection signal having a value that is indicative of the voltage appearing at the output of the output transistor (col 4 lines 1-32, col 6 lines 30-41), and further comprising:

compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, and the current output power level of the power amplifier module (col 3 lines 55-67, col 4 lines 1-32). Therefore, it would have been obvious to ordinary skill in the art at the time the invention was made to combine the above teaching of Kenji with Hadichristos, in order to provide a protection circuit for switching power amplifier which eliminates the needs for expensive transistors with high speed switching function.

Regarding **claims 2, 10**, Hadjichristos teaches a power amplifier module/method/mobile terminal as in claim 1, further comprising an impedance matching circuit coupled between the output of the output transistor and the output node, the impedance matching circuit presenting a variable impedance that is controlled by an output signal from the compensation circuitry (col 3 lines 55-67, col 4 lines 1-25).

Regarding **claims 3, 11**, Hadjichristos teaches a power amplifier module/method/mobile as in claim 2, where the output signal from the compensation circuitry is generated to have a value that is a function of the value of the first detection signal and the current output power level (col 5 lines 50-67, col 6 lines 1-5).

Regarding **claims 4, 12**, Hadjichristos teaches a power amplifier module/method/mobile as in claim 2, where the output signal from the compensation circuitry is generated when the current output power level exceeds a predetermined output power level (col 6 lines 1-42).

Regarding **claims 5, 15**, Hadjichristos teaches a power amplifier module/method/mobile as in claim 1, where the compensation circuitry makes a change to at least one of the plurality of power amplifier bias current and bias voltage

signals when the current output power level exceeds a predetermined output power level (col 6 lines 1-42).

Regarding **claims 6, 13-14, 18, 22**, Hadjichristos teaches a power amplifier module/method/mobile as in claim 2, where the compensation circuitry makes a change to at least one of the plurality of power amplifier bias current and bias voltage signals when the current output power level exceeds a first predetermined output power level (col 3 lines 35-55); and

where the output signal from the compensation circuitry to the impedance matching circuit is generated when the current output power level exceeds a second predetermined output power level that is greater than the first predetermined output power level (col 4 lines 42-60).

Regarding **claims 7, 15**, Hadjichristos teaches a power amplifier module/method/mobile as in claim 1, where the compensation circuitry controls the generation of the power amplifier bias current signal as a function of a value of the first detection signal and a value of a signal that is indicative of the current output power level (col 5 lines 50-67, col 6 lines 1-42).

Hadjichristos fails to teach controlling the generation of the power amplifier bias voltage signal as a function of a value of the second detection signal and the value of the signal that is indicative of the current output power level. However, Kenji teaches a power amplifier controlling the generation of the power amplifier bias voltage signal as a

function of a value of the second detection signal and the value of the signal that is indicative of the current output power level (col 3 lines 55-67, col 4 lines 1-32).

Therefore, it would have been obvious to ordinary skill in the art at the time the invention was made to combine the above teaching of Kenji with Hadichristos, in order to provide a protection circuit for switching power amplifier which eliminates the needs for expensive transistors with high speed switching function.

Regarding **claims 8, 16, 19, 23-24**, Hadjichristos teaches amplifier module/mobile/method as in claim 1, where the detection circuitry comprises a current mirror in parallel with the output transistor for generating the first detection signal (col 7 lines 6-24). However, Hadjichristos fails to teach a rectifier coupled to the output of the output transistor for generating the second detection signal. However, Kenji a rectifier coupled to the output of the output transistor for generating the second detection signal (col 3 lines 55-67, col 4 lines 1-32, col 6 lines 30-41). Therefore, it would have been obvious to ordinary skill in the art at the time the invention was made to combine the above teaching of Kenji with Hadichristos, in order to provide a protection circuit for switching power amplifier which eliminates the needs for expensive transistors with high speed switching function.

Regarding **claims 25**, Hadjichristos teaches a mobile radio communication terminal as in claim 21, where a signal transmitted from said antenna comprises:

a wideband code division, multiple access signal (col 1 lines 9-26).

Response to Arguments

2. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. **Any responses to this action should be mailed to:**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naghmeh Mehrpour whose telephone number is 571-272-7913. The examiner can normally be reached on 8:00- 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold be reached (571) 272-7905.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NM

May 15, 2007


NAGHMEH MEHRPOUR
PRIMARY EXAMINER